RESEARCH ARTICLE OPEN ACCESS

Voltage Controlled Oscillator

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Abstract
This paper presents the design of low power Voltage Controlled Oscillator with differential stages. Circuit uses multiple pass loop architecture having primary and secondary (auxiliary feed forward) loops. In delay cell positive feedback is used with cross coupled regenerative PMOS load, due to that power consumption reduces. For best tuning range multiple delay path is used. Measurement shows that Oscillator has linear frequency voltage characteristics. This oscillator operates at 1.8V supply. After circuit designing, 2.17GHz-4.16GHz tuning rang, 2.57 GHz centre frequency with 3mw power consumption is obtained.
Further to reduce power consumption of Voltage Controlled Oscillator, drain bulk connected PMOS load is used that works in sub-threshold region. If Bulk drain is connected it shows more linearity. By using Bulk drain connected transistor; Power Consumption reduces up to 165 μw and frequency is 1.6GHz with tuning range 1.13GHz-2.6GHz.
Keywords: Low Power, Sub threshold region, Multiple-pass loop architecture, Voltage Controlled Oscillator, Ring Oscillator

I. INTRODUCTION

Voltage Controlled Oscillator has a variety of application e.g. in communication, PLL (phase locked Loop), medical field etc. In all above mentioned applications, high frequency with low power is required. There are many ways to reduce power and to increase frequency. A Voltage Controlled Oscillator can be built by using LC Oscillator, Relaxation Oscillator or resonator circuit. In LC oscillator, at high frequencies, complexity increases due to designing of Inductors and other problems as control of eddy currents [1]. Ring Oscillator consumes less area than LC Oscillator and easy to achieve high frequency with wide tuning ranges [2]. Power consumption can be reduced in differential ring Oscillator because less number of stages can be used [3]. Use of Partial Positive feedback is also another approach to reduce power consumption [4].

Stack transistor is not efficient way to reduce power due to low swing output voltage [5]. Sub threshold is an efficient way to reduce power consumption [6]-[7]. Sub threshold operation provides more transconductance g_m for a given bias circuit and this property also can be used for a low power circuit [8]. In this paper Bulk drain connected topology is presented to work in sub threshold region [9].

Rest of the paper is organized in the following way: The architecture of multiple pass ring oscillator is discussed in Section II. Design of VCO with multiple pass stages is explained in Section III. In Section IV Bulk Drain connected VCO is discussed. In Section V, Simulation results and their comparison with other Oscillators is discussed and layout of delay cell has been presented. Section VI, presents the conclusion of work.

II. MULTIPLE PASS RING OSCILLATOR

Single loop ring Oscillator has frequency limitation, as it requires odd number of stages and propagation delay is also increased. To explore the frequency limitation of single loop ring oscillator, many techniques have been proposed [10]. In this paper multiple pass loop technique is adopted, in which two loops are used: Primary loop and secondary (an extra loop) feed forward auxiliary loop. Secondary loop works in the conjunction of Primary loop. Primary Input of each stage is connected to the differential output of previous stage. Secondary Input of each stage is connected to the primary input of previous stage with a phase shift of 180^0 . Figure 1 shows the architecture of multiple pass ring oscillator.

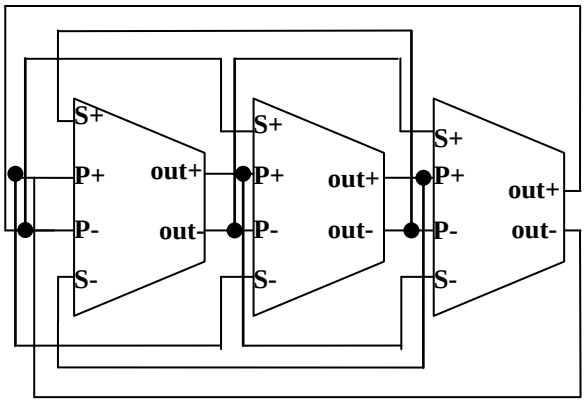


Figure 1. Multiple Pass Ring Oscillator with Primary and secondary loop

III. Design Of Voltage Controlled Oscillator

To Design a Voltage Controlled Oscillator using Multiple Pass loop with different delay cells are discussed [11]. An approach for a wide tuning range, with low power, partial positive feedback is used. Due to positive feedback, Oscillations enhances, thus less power consumption takes place. Another approach use of differential amplifier in parallel [12], increase frequency of oscillations but in that case power consumption is very high because of many parallel stages of PMOS load.

In this paper Voltage Control Oscillator with full swing output, with three delay stages is designed. Schematic of delay cell is shown in Figure 2. This cell is designed using differential stages to reduce the common mode noise. In this cell multiple delay paths with positive feedback is used. M_3-M_4 form positive feedback loop, due to that switching speed of cell decreases and Power consumption also reduces. M_5-M_6 carry different delay path. Due to these paths tuning range of Oscillator can be varied by changing their width respective to each-other. M_7-M_8 is connected to primary inputs.

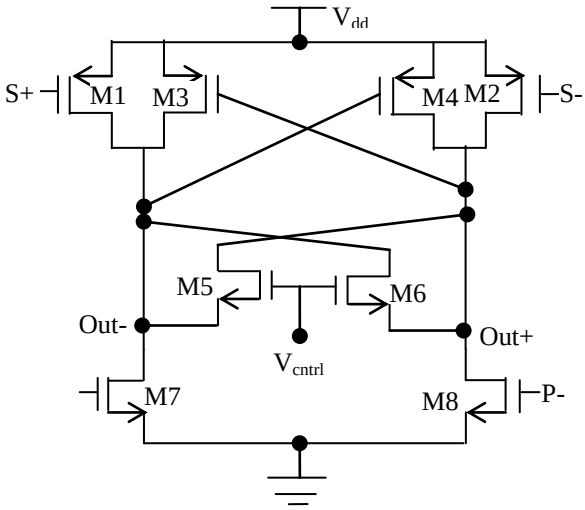


Figure2. Delay Cell of ring VCO

IV. Design Of Voltage Controlled Oscillator in Sub Threshold Region

Sub threshold device operates at such voltage that is less than its threshold voltage. To make a circuit working in sub threshold region, there are many techniques provided earlier [4],[6],[9]. Important feature of Sub threshold is low power. Power has a quadratic relation with voltage supply. In strong Inversion, circuit operates at high voltage, so correspondingly more power consumption.

In this paper Bulk Drain Connected PMOS load is used to operate circuit in sub threshold region. In CMOS, p-substrate technology, only Load PMOS devices can be used for a bulk drain connection because of their implementation in n-well [4]. Conventionally PMOS devices require large resistance in triode region, accordingly large channel length. By connecting Bulk drain, I-V curve shows more linearity [4] that can be used for sub threshold operation.

Delay cell of Voltage Controlled Oscillator using bulk drain connected PMOS device is shown in figure 3. In this circuit M_2-M_5 and M_7-M_8 forms multiple delay paths with positive feedback. M_3-M_4 is used for complementary control voltage to increase the frequency and to overcome the limitations of low control voltage.

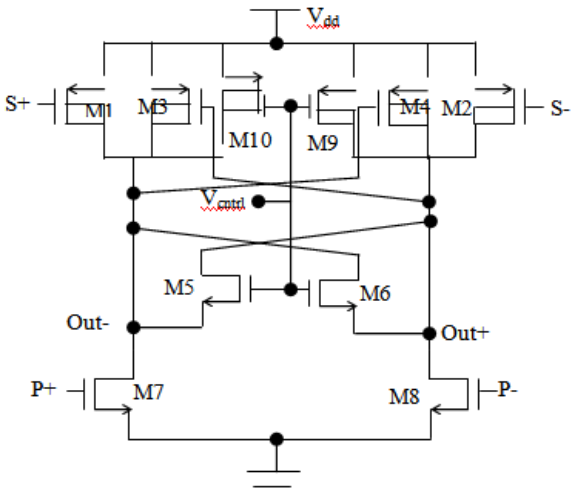


Figure3. Delay cell of Ring Oscillator VCO in Sub threshold region

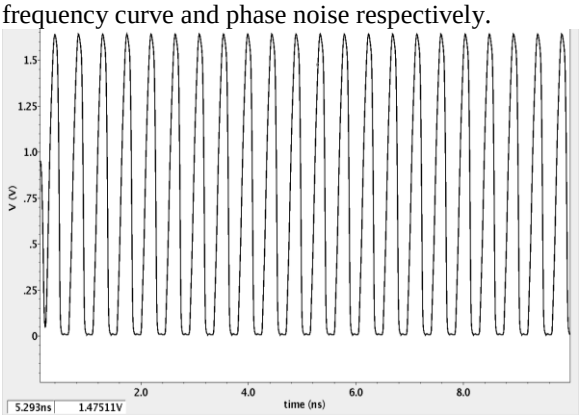
V. Result Of Voltage Controlled Oscillator in Sub Threshold Region

Performance of VCO circuit is simulated using BSIM of 180nm and compared with other existing VCO.

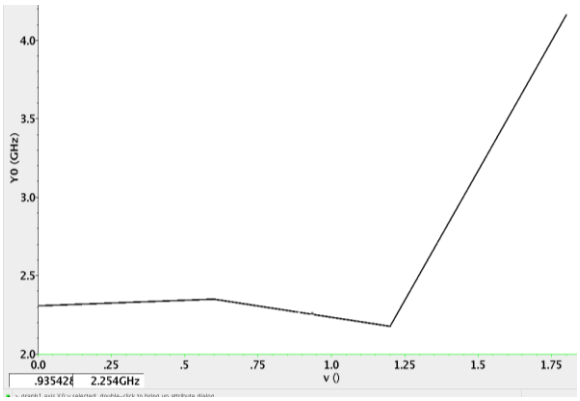
After simulation of Voltage Controlled Oscillator in strong inversion region, frequency of 2.57GHz is obtained and tuning range is 2.17GHz. Phase Noise is -97dBc/Hz @1MHz offset frequency.

Power consumption is 3mw. Figure 4(a), 4(b), 4(c) shows transient analysis, Voltage frequency curve and phase Noise respectively. From Figure 4(b) it can be concluded that Frequency of Oscillator increases with the increase in voltage. It follows linear relationship between voltage and frequency.

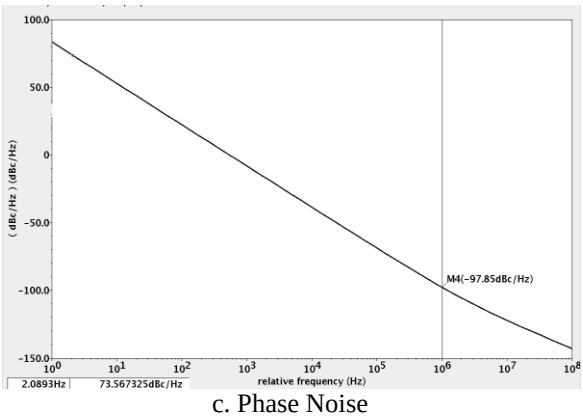
Further, Simulating VCO in sub threshold region, frequency of 1.6 GHz. is achieved with a tuning range of 1.3GHz-2.6GHz. Phase Noise is -89dBc/Hz @1MHz offset frequency. Power Consumption is 165 μw. Figure 5(a), 5(b), 5(c) shows the response of transient analysis and voltage frequency curve and phase noise respectively.



a. Transient Analysis

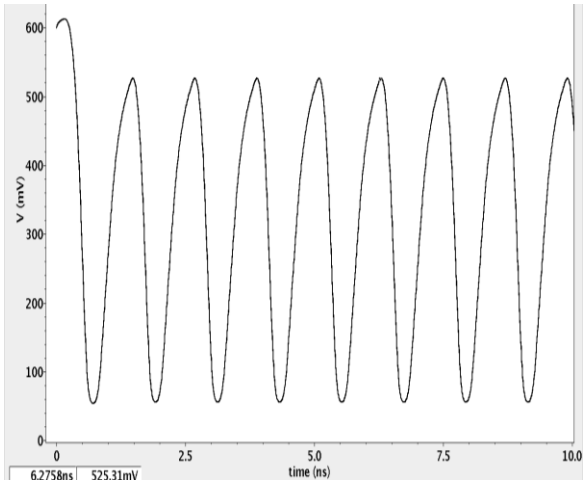


b. Voltage Frequency Curve

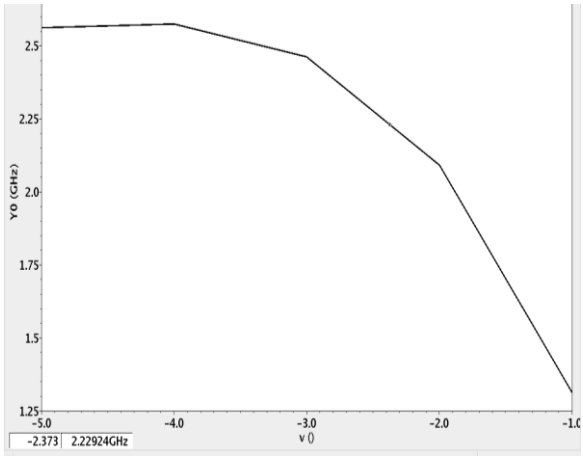


c. Phase Noise

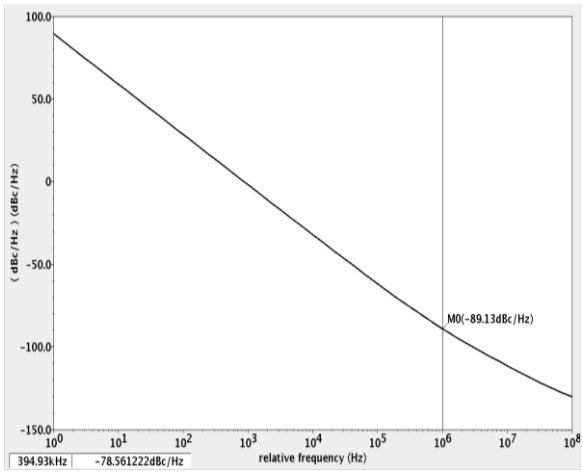
Figure 4: Analysis of VCO using conventional load PMOS



a. Transient Analysis



b. Voltage Frequency Curve



c. Phase Noise

Figure 5: Analysis of VCO using Bulk Drain connected load PMOS

Later on, VCO with conventional PMOS load is compared with already existing VCO.

TABLE I
COMPARISON WITH EXISTING VCO

Parameters	[12]	[4]	This Work
Supply Voltage (v)	1.8	1.5	1.8
Tuning Range (MHz)	186-1576	130-3510	2170-4162
Power Consumption (mw)	18.95	4.98	3
Output Swing (v)	-	-	1.8

Layout of the Delay cell in sub threshold region has shown in figure 6.

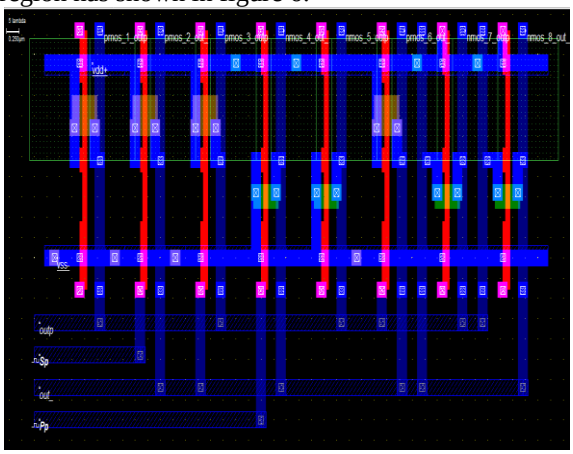


Figure 6: Layout of Delay cell of VCO

VI. CONCLUSION

In this paper low power voltage controlled oscillator with wide frequency range, full swing output voltage is designed and simulation is done by using cadence (RF Spectrum), gpdk 180 nm technology. In Conventional method, positive feedback is used to reduce power consumption.VCO with conventional load consumes only power 3mw power with a wide tuning range 2.17GHz-4.16GHz and applied power supply is 1.8V. Simulations shows that this VCO gives full swing voltage output.. These characteristics can be used for Low power application. Further to reduce power, circuit is designed in Sub threshold region by connecting Bulk-drain of Load PMOS. In sub threshold region, power consumption reduces up to165 μw with tuning range 1.3GHz-2.6GHz.These characteristics can be used for ultra low power Medical applications.

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